METHOD AND APPARATUS FOR ENSURING SYNCHRONIZATION OF CLOCKS IN A MULTIPLE CLOCK SYSTEM

ABSTRACT

An apparatus, a method, and a computer program product are provided for producing a synchronous divider reset signal. A notorious concern with multiple non-integer frequency ratio synchronous source clocks has been the time of edge alignment between the respective clocks. To address this concern, a number of latches can be utilized in order to detect alignment of the edges of these clocks. Specifically, the latches are employed to assist in the production of a synchronous divider reset signal for downstream dividers that are utilized in many microprocessors today. Hence, all of the downstream dividers can be properly synchronized to alleviate any errors that can occur between respective macros of a microprocessor chip resulting from misalignment of clock edges.